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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR, LTD., a Bermuda corporation; and ALPHA & OMEGA SEMICONDUCTOR, INC., a California corporation,

Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR CORP., a Delaware corporation,

Defendant and Counterclaimant.

AND RELATED COUNTERCLAIMS.

Case No. C 07-2638 JSW
(Consolidated with Case No. C-07-2664 JSW)

AOS'S OPENING CLAIM CONSTRUCTION BRIEF PURSUANT TO PATENT L.R. 4-5

Date: June 4, 2008
Time: 2:00 p.m.
Location: Courtroom 2, 17th Floor
Judge: Hon. Jeffrey S. White

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I. INTRODUCTION

Plaintiffs Alpha & Omega Semiconductor, Ltd. and Alpha & Omega Semiconductor, Inc. (collectively, "AOS") assert that defendant and counterclaimant Fairchild Semiconductor Corp. ("Fairchild") infringes three AOS patents. The inventions taught and covered within these patents dramatically improved the performance of power MOSFETs, which are transistors used in a wide variety of electrical devices. The power MOSFET market is highly competitive, and dominated by a small number of mega-companies, including Fairchild.

The following is the claim construction brief of AOS concerning Patent Nos. 5,767,567 ("567"), 5,907,776 ("776") and 5,930,630 ("630"). As discussed below, AOS has construed the claim terms in a way consistent with the patent law and the understanding of one of ordinary skill in the art.

By contrast, in an attempt to avoid a finding of infringement, Fairchild seeks to unduly narrow the constructions of key claim terms. For some terms, Fairchild improperly imports limitations from the embodiments of the specification into the claims. Alternatively, Fairchild's proposed constructions add limitations without support in the specification, patent file history, or any technical reference.

In contrast, AOS follows the Federal Circuit's guidance and proposes a construction for each of the disputed terms[1] that adopts the plain meaning of the claim language, reflects how the terms would be understood by a person of ordinary skill in the art, and is consistent with the specifications and file histories of the patents. Rather than simply limit the claims to the embodiments disclosed in the specifications, AOS offers an analysis of how the words of the claims would be understood when considered in light of the entire intrinsic record, including the problems solved by each of the asserted patents. By applying the proper claim construction analysis, AOS proposes constructions that are faithful to the claimed inventions and comport with the actual patent contributions.

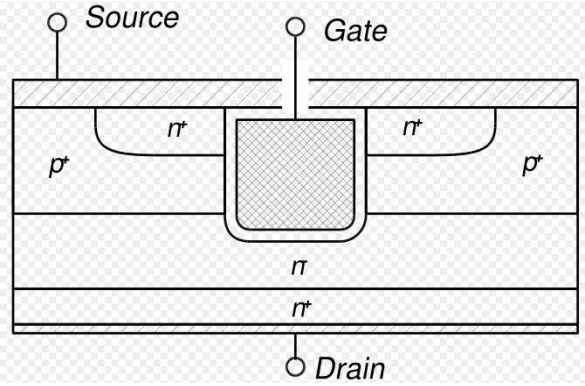
[1] The current briefing addresses the ten highest priority disputed claim terms selected by the parties. In this opening brief, AOS addresses only the four terms that appear in the AOS patents. AOS will address the six disputed terms in Fairchild's patents in AOS's opposition brief.

II. BACKGROUND

A. AOS And Its Pioneering Patents

AOS is a success story in the semiconductor industry and the Silicon Valley. AOS was founded in September 2000, by seven engineers with over 120 years of combined experience in the semiconductor industry. Headquartered in Sunnyvale, California, AOS designs power MOSFET products, but owns no fabrication facility (AOS is "fabless"). AOS first generated revenue from product sales in 2001, and became profitable the next year. AOS is now among the fastest growing competitors in the discrete power MOSFET market. In this litigation, AOS asserts three patents originally developed by MegaMOS Corporation ("MegaMOS") and assigned to AOS.

B. Overview of Power MOSFET Technology



To understand properly the innovations of the AOS patents-in-suit, a brief and high level overview of power MOSFET technology may be helpful to the Court.

A power MOSFET is an electronic switch, commonly used in devices such as cell phones and laptop computers. A power MOSFET comprises many, typically millions, of individual transistor "cells" working together to switch large amounts of power on and off. Generally, the inventions of the AOS patents-in-suit improve the performance of power MOSFETs by (1) reducing resistance to the flow of electrical power, and (2) reducing the voltage required to turn the devices on, while (3) not decreasing the amount of power the devices can handle.

A power MOSFET is a type of transistor. The basic structure of a transistor is that it typically has three terminals: a gate terminal, a source terminal and a drain terminal. The basic objective of a transistor is to pass electricity between the source and the drain on command. In effect the transistor turns on and off allowing current to pass. Typically the **gate** receives a control signal that will turn on the transistor. A power signal is received at the input side, the

source, and passes through a channel, a region next to the **gate**, and then passes to the drain. The power signal is then discharged by the drain to another device that is connected to the power MOSFET.

Resistance to the flow of power may be affected by the path through which current flows when the device is turned on. This is the "on-state resistance" of the device, also called R_{DSON}. The farther current must travel through the power MOSFET, the more power is lost due to the natural resistance of the semiconductor material through which the current passes. Declaration of Andrew J. Wu, submitted herewith, Ex. 1 ("Wu Ex. 1"), '567 patent, col. 1:16-24.

The voltage required to turn on a power MOSFET is called the "threshold voltage," also called V_{TH}. A lower threshold voltage allows the MOSFET to be switched on and off faster and to be used in smaller products with increased battery life. *Id.*, at cols. 1:16-25; 4:5-8.

The voltage that a power MOSFET can handle before it fails is called the "breakdown voltage," sometimes called V_b. When voltage exceeding V_b is applied, the device fails and very large amounts of power will flow even though the device should be turned off. For decades, researchers have attempted to reduce the on-state resistance or power consumption of MOSFETs without undesirably reducing breakdown voltage.

The AOS Patents in suit improve power MOSFET quality in at least three ways. The '567 patent reduces a power MOSFET's on-state resistance without decreasing breakdown voltage (V_b) by connecting the power MOSFET to its packaging in a way that shortens the path through which power must flow when the device is turned on. The '630 patent reduces a power MOSFET's resistance without decreasing the breakdown voltage through an improved contact and a simplified fabrication process. The '776 patent reduces a power MOSFET's threshold voltage without decreasing V_b by reducing the amount of charge in the material along the current path of the device.

III. INTERPRETATION OF DISPUTED TERMS

A. Summary of Applicable Law

The interpretation of patent claims is a question of law to be decided by the Court. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 371-73 (1996). To interpret the claims of

a patent, the Court must consider the language of the claims, the specification, and the prosecution history. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995), *aff'd*, 517 U.S. 370 (1996). In construing a claim, the court must first look to the specific words of a claim. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005). The words of a claim are generally given their ordinary meaning, unless it is apparent from the patent and the prosecution history that the inventor used the term with a different meaning. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). The court must interpret the claims in view of the specification which "is the single best guide to the meaning of a disputed term." *Id.*

The Federal Circuit has repeatedly warned, however, that claims should not be limited to the embodiments disclosed in the specification. *See Phillips*, 415 F.3d at 1323; *Renishaw PLC v. Marposs Societa' Per Azioni*, 158 F.3d 1243, 1248 (Fed. Cir. 1998); *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1340 (Fed. Cir. 2001) (describing "one of the cardinal sins of patent law - reading a limitation from the written description into the claims.") At the other extreme, a claim construction that would exclude a preferred embodiment is rarely, if ever, correct. *Vitronics*, 90 F.3d at 1583-4.

The words used by a patent should be construed to be consistent throughout the patent. *Phillips*, 415 F.3d at 1314; *see also Southwall Tech., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1579 (Fed. Cir. 1995). The varied use of a disputed term "attests to the breadth of a term rather than providing a limiting definition." *Anchor Wall Sys., Inc. v. Rockwood Retaining Walls, Inc.*, 340 F.3d 1298, 1308-09 (Fed. Cir. 2003).

The doctrine of claim differentiation creates a presumption that each claim in a patent has a different scope. *Kraft Foods, Inc. v. Int'l Trucking Co.*, 203 F.3d 1362, 1368 (Fed. Cir. 2000). Hence, claim differentiation generally will prevent reading a limitation found in one claim into another claim if that "limitation is the only meaningful difference between the two claims." *Wenger Mfg., Inc. v. Coating Machinery Sys., Inc.*, 239 F.3d 1225, 1233 (Fed. Cir. 2001). *See also Phillips*, 415 F.3d at 1324-25 (holding that the "baffles" in a claim did not inherently include the limitations of other dependent and independent claims).

B. The '567 patent

The invention of the '567 patent decreases on-state resistance and therefore wasted energy in power MOSFETs by shortening the path through which current must flow when the device is on.

1. The Invention Of The '567 Patent

Power MOSFETs are encased within plastic packages, and a power MOSFET is connected to its packaging through one or more wires, called "lead wires." These lead wires connect a lead frame of the packaging to "source contact areas" in the surface of the power MOSFET.

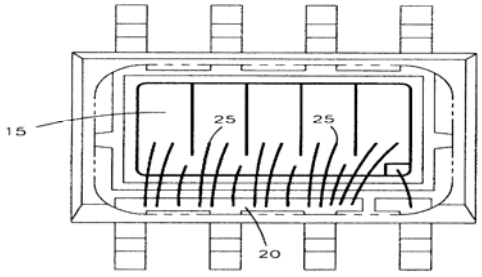


FIG. 1A
(PRIOR ART)

The "source contact area" is the surface of the power MOSFET to which power is applied, and to which the lead wires are connected. '567 patent, col. 1:37-47. Typically located on the top of the device, it provides a surface for connecting to each of the potentially millions of individual transistor cells comprised by the MOSFET device. The source contact area may be divided into multiple sub-contact areas by structures called "gate runners." *Id.* "Gate runners" are stripes of conductive material. For example, Figure 1A of the '567 patent (above) shows at least four gate runners that extend across the die surface. These four gate runners create five sub-contact areas. *Id.* The gate runners connect the gates to a gate voltage supply.

In MOSFET designs prior to the '567 patent, significant energy was wasted due to the connection of the power MOSFET to its external packaging. To lessen the expense and ease manufacturing, the prior art, shown in Figure 1A of the '567 patent, arbitrarily connected short lead wires (25) to the region of the contact areas close to the lead frame (20). As a result, current flowing through transistor cells that are remote from the lead wire contacts has to travel across the source contact area for a long path before reaching the conductive lead wires. '567 patent, col. 1:37-65. Since the resistance along a current path is proportional to the distance the current must travel, the longer current path in the prior art designs led to more resistance, and hence more

wasted energy.

The '567 patent invention reduces on-state resistance, R_{DSON}, by distributing the lead wires over the source contact area of the device and spreading the points of contact for the lead wires over the contact area. '567 patent, Abstract, col. 2:29-34, col. 5:1-14. The '567 patent describes several approaches to this distribution, including distributing the lead wires so that the number of lead wires is proportional to the contact area. *E.g.,* '567 patent at col. 3:67-col. 4:60. This aspect of the invention is recited in claim 7, which AOS asserts against Fairchild.

Claim 7 of the '567 patent recites as follows:

> 7. A method to configure a source contact area on a power MOSFET device by dividing said source contact areas with several gate runners disposed thereon, said method including steps of:
>
> (a) determining a total number of lead wires for connecting to a lead frame from said source contact area on said MOSFET power device; and
>
> (b) configuring said gate runners for dividing said source contact area into several sub-contact areas with a set of area proportional ratios for disposing several of said lead wires in each of said sub-contact areas according to said set of area proportional ratios.

Wu Ex. 1, '567 patent. The disputed terms are highlighted in blue and green.

2. "Several" is used in the specification to mean "two or more."

Disputed Term	**AOS's Proposed Construction**	**Fairchild's Proposed Construction**
Several	Two or more	Three or more

AOS's proposed construction of "several" is consistent with the inventors' use of that term in the specification. Throughout the claims and the specification, the '567 patent uses the words "several" and "plurality" to describe the number of gate runners, sub-contact areas, lead wire contacts within a sub-contact area, and so on. The '567 patent's use of "several" within the specification and claims requires that it be construed as "two or more."

Construing "several" to mean "three or more" – Fairchild's proposed construction –

would be inconsistent with the specification. Describing Figs. 2C and 2D, the '567 patent discloses a method to configure the source contact area of a power MOSFET including "disposing several of the lead wires . . . in each of the sub-contact areas." '567 patent, col. 5:54-55.[2] As Fig. 2C of the '567 patent shows, the right-most sub-contact area 150-4 contains only two lead wires. (Note that the short third wire at the lower right corner of the device connects the lead frame G to the gate contact area, which is separate from the source contact area. Declaration of C. Andre T. Salama, submitted herewith ("Salama Decl.") ¶ 2. If "several" means "three or more" as Fairchild proposes, the patent's statement that Figures 2C and 2D depict several lead wires in each source sub-contact area would be incorrect. '567 patent, col. 5:54-55. Indeed, Fairchild's proposed definition would exclude this preferred embodiment from the claims and so must be rejected. *See Vitronics*, 90 F.3d at 1583-4.

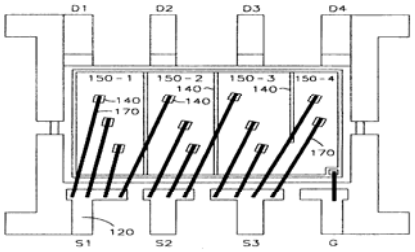


FIG. 2C

Further, the term "several" must be construed to mean the same thing as "plurality," because the specification of the '567 patent uses the terms "several" and "plurality" interchangeably to describe the same elements in the same figure. For example, the specification alternately describes both Figs. 2C and 2D as containing "a plurality of gate runners . . . disposed on the source contact area," *Id.*, col. 5:37-40, and "source contact areas . . . with several gate runners . . . disposed thereon," *Id.*, col. 5:45-53 Likewise, the specification describes gate runners in Fig. 3 of the '567 patent that "divide the source contact area into a plurality of sub-regions." Col. 5:60-62 But the next paragraph describes the gate runners in Fig. 3 as "dividing the source contact area into several sub-contact areas." *Id.*, col. 6:15-18. Because the patent uses the terms "several" and "plurality" interchangeably, "several" should be construed to have the same meaning as "plurality" – two or more. In patent claims, a "plurality" means simply "more than one." *See, e.g., Bowers v. Baystate Techs., Inc.*, 320 F.3d 1317, 1332 (Fed. Cir. 2003) ("The claim, however, uses the term 'plurality,' meaning 'comprising, or consisting of more than

[2] Throughout this brief, any emphasis in quoted material was added to the original text, unless stated otherwise.

one.'").

AOS's proposed definition is also consistent with the plain meaning of "several," as evidenced by dictionary definitions. Merriam Webster's Collegiate Dictionary defines "several" as "more than one." Wu Decl. Ex. 5 at 1073. The Oxford English Dictionary states that "in legal use" the word "several" means "more than one." Wu Decl. Ex. 4 at 4. The Microsoft Encarta Collegiate Dictionary states that "several" is just "a grammatical word indicating a small number"). Wu Decl. Ex. 6 at 1324. To the extent Fairchild tenders dictionaries that define "several" differently, those definitions are inconsistent with the patent specification and must be rejected. *See Phillips*, 415 F.3d at 1322-23 (holding that judges are free to consult dictionaries at any time, "so long as the dictionary definition does not contradict any definition found in or ascertained by a reading of the patent documents").

3. "Configuring said gate runners for dividing said source contact area into several sub-contact areas with a set of area proportional ratios"

Disputed Term	AOS's Proposed Construction	Fairchild's Proposed Construction
Configuring said gate runners for dividing said source contact area into several sub-contact areas with a set of area proportional ratios	**The placement of gate runners divides the source contact area into sub-contact areas, and a set of area proportional ratios are defined by the ratios of the approximate areas of the sub-contact areas.**	**Arranging the gate runners, after determining the total number of lead wires, to define several sub-contact areas that are not all equal in size and such that the ratio of lead wires to area is the same for each of the sub-contact areas.**

The plain language of claim 7 of the '567 patent states that the placement or arrangement of the gate runners divides the source contact area into sub-contact areas. The plain language states that the area proportional ratios of the sub-contact areas are the ratios of the sub-contact areas. Configuring the gate runners simply refers to placing the gate runners to divide the source contact area into sub-contact areas in accordance with the other limitations of this claim element. *See* '567 patent, col. 2:43-49, col. 5:45-57. Since this is the plain meaning of the claim language, this is where AOS's proposed construction ends.

Fairchild's proposed construction, on the other hand, would add three limitations not present in the plain language of the claim and would require a mathematical precision inconsistent with the preferred embodiments disclosed within the '567 patent itself.

a. Fairchild's proposed limitation "after determining the total number of lead wires"

Although claim 7 of the '567 patent includes two steps, the claim language does not impose any order in which the steps must be performed, and does not require that the step of determining the number of lead wires must be performed prior to the step of configuring the gate runners. It is settled that the steps in a method patent claim need not be performed in the order recited. *Interactive Gift Express, Inc. v. Compuserve, Inc.,* 256 F.3d 1323, 1343 (Fed. Cir. 2001) ("[u]nless the steps of a method actually recite an order, the steps are not ordinarily construed to require one.") Here, the preamble of claim 7 recites only that both steps must be "include[ed]." '567 patent, col. 8:36-37.[3] One step consists of:

> determining a total number of lead wires for connecting to a lead frame from said source area on said MOSFET power device

Id., col. 8:38-40. This step does not mention any other step, does not explicitly or implicitly require any sequence of performance, and does not implicitly depend on any other step for its own performance. The other step consists of:

> configuring said gate runners for dividing said source contact area into several sub-contact areas with a set of area proportional ratios

Id., col. 8:41-43. This operation also does not mention any other step, does not explicitly or implicitly require any sequence of performance, and does not implicitly depend on any other step for its own performance. It is not necessary from a technical standpoint, to have determined the number of lead wires in order to configure the gate runners. The disputed claim element "configuring the gate runners . . . with a set of area proportional ratios" does not depend on the determination of the number of lead wires; the number of lead wires could just as readily be determined after the configuration of the gate runners. Nothing in the plain language of claim 7

[3] In addition, the usage of "including" is the same as "comprising," creating an open-ended list of elements. *Hewlett-Packard Co. v. Repeat-O-Type Stencil Mfg. Corp., Inc.*, 123 F.3d 1445, 1451 (Fed. Cir. 1997) (holding that "[t]he claim term 'including' is synonymous with 'comprising'").

supports Fairchild's proposal that the gate runners must be arranged "after" determining the total number of lead wires.

Moreover, because unasserted claim 8 of the '567 patent explicitly imposes a sequence for performing the same two operations, claim differentiation dictates that that sequence should not be imposed on claim 7. *See, e.g., Wenger Mfg., Inc.*, 239 F.3d at 1233. Claim 8, unlike claim 7, requires "configuring said gate runners according [to] said total number of lead wires. . . ." *Id.*, col. 8:55-56. The determination of the lead wires in claim 8 must occur first because the configuration of the gate runners in claim 8 is made "according to" that number. Therefore, the configuration of gate runners can occur either before, after, or at the same time as the determination of the number of lead wires is determined for purposes of claim 7.

b. Fairchild's proposed limitation "not all equal in size"

Another of Fairchild's proposed additions to the plain language of the disputed phrase is a requirement that the sub-contact areas are "not all equal in size." This limitation is not only unsupported by the intrinsic evidence, but the '567 patent and the canon of claim differentiation both contradict Fairchild's proposed limitation.

Equations in the specification explicitly allow all of the sub-contact areas to have the same size. The '567 patent teaches dividing the lead wires among the sub-contact areas. If the division occurs evenly, then each sub-contact area has the same number of wires and the same size. That situation is expressly permitted in the '567 patent, establishing that all of the sub-contact areas may have the same size.

To explain the distribution process, the specification of the '567 patent introduces the variables N_{LW}, the number of lead wires, and N_{GR}, the number of gate runners. '567 patent, col. 4:25-36. The number of sub-contact areas is $N_{GR} + 1$.[4] *Id.* N_{BASIC}, is the integer quotient of dividing N_{LW} by $N_{GR} + 1$ (*i.e.*, distributing the lead wires among the sub-contact areas). The specification notes that there may be a remainder, $N_{REMAINDER}$, which is the number of lead wires left over after distributing an equal number of lead wires to each sub-contact area:

[4] With one gate runner, there are two sub-contact areas, and so on. The number of sub-contact areas is generally one more than the number of gate runners.

$$N_{LW} = (N_{GR}+1) \times N_{BASIC} + N_{REMAINDER}$$

Id. For example, if you divide 7 by 3, you get a quotient of 2 and a remainder of 1. That is, 7 = 3 × 2 + 1. Similarly, dividing 14 by 3 yields a quotient of 4 and a remainder of 2. That is, 14 = 3 × 4 + 2. As a final example, 3 divides into 15 evenly, so the remainder is zero: 15 = 3 × 5 + 0. As these examples show, the remainder is zero when the division occurs evenly.

The specification explicitly states that the remainder $N_{REMAINDER}$ can be zero at col. 4:33-36. When the remainder is zero, all of the sub-contact areas have the same size and the same number of lead wires. Without more, this requires rejection of Fairchild's proposed construction.

Further, because the limitation of "different size sub-contact areas" appears in other claims besides claim 7, the principle of claim differentiation once again prohibits importation of this limitation into claim 7. *See, e.g., SRI Int'l v. Matsushita Electric Corp. of Am.*, 775 F.2d 1107, 1122 (Fed. Cir. 1985) ("[i]t is settled law that when a patent claim does not contain a certain limitation and another claim does, that limitation cannot be read into the former claim in determining either validity or infringement."). The limitation of different size sub-contact areas appears in claims 1, 5, and 6 – but not in claim 7.

c. Fairchild's proposed limitation "is the same for each sub-contact area"

Fairchild also proposes to create from whole cloth an additional requirement that "the ratio of lead wires to area is the same for each of the sub-contact areas." Nowhere in the phrase to be construed are lead wires even mentioned. Nor does the rest of claim 7 discuss the "ratio of lead wires to area." Indeed, the distribution of the lead wires is determined by the ratio of the sub-contact areas to each other, not by the ratio of lead wires to sub-contact areas. *Id.*, col. 8:41-45. The claim language describes an area proportional ratio, not an area-to-lead wire ratio.

Even if the ratios were area and lead wire based, Fairchild's proposed requirement that the ratio be the "same" for each sub-contract area must be rejected. The figures and specification of the '567 patent demonstrate that the set of area proportional ratios is defined by the approximate areas of the sub-contact areas, without mathematical precision. For example, the specification describes the prior art Figs. 1A and 1B as dividing the source contact area into "equally divided

areas." That is, with an area proportional ratio of 1:1. '567 patent, cols. 1:43-44; 2:3-4. However, the sub-contact areas in these figures plainly are not equal; they are merely approximately equal. The rightmost sub-contact region in Fig. 1A has a small area cut out of it to supply space for the gate contact region. *Id.*, Fig. 1A. Similarly, the left-most sub-contact area in Fig. 1B has a small area cut out of it to supply space for the gate contact region. *Id.*, Fig. 1B. The same can also be seen in each of the other embodiments. The Court's construction must allow the set of area proportional ratios to be defined by the ratios of the approximate areas of the sub-contact areas - otherwise, the preferred embodiments themselves would be excluded. *See Vitronics*, 90 F.3d at 1583-4.

C. The '630 Patent

1. Background and Summary of the '630 Patent

The structure of a power MOSFET is created during the fabrication process through a sequence of operations that build the device, step by step, atop a silicon wafer substrate. These operations may include steps such as depositing layers of different materials on the substrate, doping regions of the device with charged particles, or etching away portions of the substrate to define desired physical structures.

Many of these operations require a "mask." A mask is simply a stencil that covers certain areas and leaves others open. Like a painter using a stencil to define an area in which to paint, a semiconductor manufacturer applies masks to the surface of the unfinished MOSFET to define areas that will be subjected to various operations during fabrication. Salama Decl. ¶ 5.

Openings in the mask expose areas of the substrate that are then etched. "Etching" is one of the operations used to form physical structures in a power MOSFET. Etching removes layers of material through certain chemical or physical processes. Material covered by the mask will not be removed; material left exposed by the mask will be etched away. Salama Decl. ¶¶ 4, 5.

One of the physical structures defined during fabrication is the "gate." As discussed earlier, the gate is the structure that turns a transistor on when a voltage exceeding the threshold voltage, V_{TH}, is applied to the gate. Gates can be either "planar" or "trenched." A planar gate sits on top of the substrate. A trenched gate extends downward into the substrate. Salama Decl. ¶¶ 6,

7.

The invention of the '630 patent improved over the prior art in at least two ways. Generally, the '630 patent avoids the need for a separate masking step that had been required in the prior art processes by using as a mask the insulation layers covering the gates. *E.g.,* '630 patent, col. 4:24-34 ("insulation layers covering the gates are employed as ion-blocks for body implants … whereby the requirements of additional masks or sidewall spacers as that employed in the prior art are no longer necessary"). This process is recited in claim 1 of the '630 patent. Also, the invention of the '630 patent provides a source contact structure with reduced on-state resistance in the contact to the source regions, by removing the top portion of the source contact region to reduce the device's contact resistance. *E.g.,* '630 patent, col. 4:5-9. This aspect of the invention is recited in claim 3 of the '630 patent.

Claim 1 of the '630 patent recites as follows:

> **1**. A method for fabricating a MOSFET transistor on a substrate comprising steps of:
>
> a) forming an epi-layer of a first conductivity type as a drain region in said substrate and then growing an initial oxide layer over said epi-layer;
>
> (b) applying an active mask for etching said active layer to define an active area followed by depositing an overlaying polysilicon layer thereon and applying a polysilicon mask for etching said polysilicon layer to define a plurality of polysilicon gates;
>
> (c) removing said polysilicon mask then carrying out a body implant of a second conductivity type followed by performing a body diffusion for forming a plurality of body regions;
>
> (d) applying a source blocking mask for implanting a plurality of source regions in said body regions with ions of said first conductivity type followed by removing said source blocking mask and a source diffusion process;
>
> (e) forming an overlying insulation layer covering said MOSFET device followed by applying a contact mask to open a plurality of contact openings there-through; and
>
> (f) performing a low energy body-dopant implant and high energy body dopant implant to form a self-aligned shallow high concentration body dopant region and a self-aligned deep high concentration body dopant region.

Wu Ex. 3, '630 patent. The disputed term is highlighted in yellow.

2. The Disputed Phrase "applying a polysilicon mask for etching said polysilicon layer to define a plurality of polysilicon gates" need not be construed.

Disputed Term	AOS's Proposed Construction	Fairchild's Proposed Construction
Applying a polysilicon mask for etching said polysilicon layer to define a plurality of polysilicon gates	**The meaning of this phrase is clear and unambiguous to a person of skill in the art, and thus it need not be construed by the court.**	**Applying a mask having a plurality of openings to allow the removal of areas of a polysilicon layer to form a plurality of polysilicon gates corresponding to the plurality of areas of the mask which are not open.**

The phrase "applying a polysilicon mask for etching said polysilicon layer to define a plurality of polysilicon gates" has a clear meaning to a person of skill in the art of power MOSFET devices, and is supported by the specification. '630 patent; Salama Decl. ¶ 3. As discussed above, a mask is used as a stencil during the etching of polysilicon material. Following the etching, polysilicon gates are defined. This claim element includes three phrases, each of which is clear enough that the additional construction proposed by Fairchild is unnecessary and inappropriate. Moreover, the purpose and effect of Fairchild's proposed construction would be to exclude all trenched-gate devices—including a preferred embodiment of the '630 patent—from the scope of the claims. Therefore, even if the Court were to construe the claim element, Fairchild's proposed construction must be rejected.

a. "applying a polysilicon mask"

This phrase has a plain meaning, and there is no suggestion in the claim language or intrinsic evidence that the phrase should include the additional limitations proposed by Fairchild that the mask "have a plurality of openings to allow the removal of areas of a polysilicon layer to form a plurality of polysilicon gates." Like the painter's stencil, a semiconductor wafer fabricator uses masks to isolate areas subject to various fabrication operations. Salama Decl ¶¶ 4, 5. Typically, a series of masks and associated etching operations are required to fabricate a power MOSFET. *Id.* The '630 patent identifies one of the masks as a "polysilicon mask" because the mask isolates portions of a previously-formed polysilicon layer that will be etched. Masking is a

basic, routine operation common to all semiconductor wafer fabrication, well understood by persons skilled in the art. *See* '630 patent, col. 7:11-23.

b. "etching said polysilicon layer"

Likewise, this phrase has a plain meaning and should not be construed to include the additional limitations proposed by Fairchild. Etching refers to removal of at least some of the polysilicon material through a chemical or physical process. Both AOS and Fairchild use etching in the fabrication of power MOSFETs, and there appears to be no dispute about what constitutes etching. Salama Decl. ¶ 4. Before etching, a mask covers part of a layer of material previously formed on the substrate surface. *Id.* Etching then removes material from the areas that are not covered by the mask. *Id.* Because etching has a well-defined meaning that is not in dispute, there is no reason to replace the concise claim language with Fairchild's proposed phrase "having a plurality of openings to allow the removal of areas of a polysilicon layer."

c. "to define a plurality of polysilicon gates"

This phrase also has a plain meaning. A layer of polysilicon material is etched so that some of the polysilicon is removed, and the polysilicon that is not removed becomes the polysilicon gates. '630 patent, col. 7:11-16. Defining gates in planar-gate and trenched-gate power MOSFETs are standard operations common to semiconductor wafer fabrication.

A planar gate is defined by its horizontal dimension. Salama Decl ¶ 7. To the right is an example showing a portion of Fig. 5B of the '630 patent. Rectangle 125 is a gate. Prior to etching, there was material to the left and the right of this gate, and the mask covered the gate. Etching removed the excess material to the left and right of the mask, thus defining the gate's horizontal dimensions. *Id.*

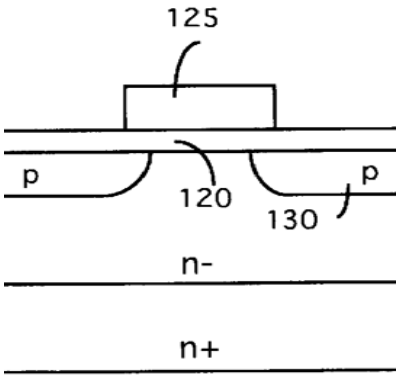
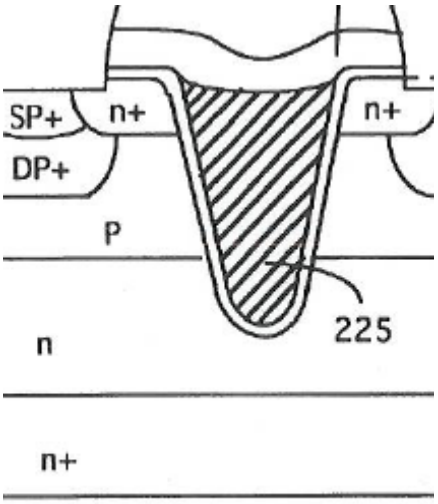


FIG. 5B

In a trenched-gate device, by contrast, a gate is defined by its vertical dimension. *Id.* To the right is an

example showing a portion of Fig. 6 of the '630 patent. The portion labeled 225 is a trenched gate, shown here at a later stage in fabrication. Prior to etching, there was polysilicon "gate" material that extended further vertically. A mask covered other regions of the substrate, so that it only exposed the gate. Etching removed the excess gate material from the substrate surface above the trench, thus defining the gate's vertical dimension. *See* '630 patent, Fig. 6.



Defining planar or trenched polysilicon gates through these etching processes is basic to semiconductor wafer fabrication and well understood by persons of skill in the art. Salama Decl. ¶¶ 3-5, 7.

d. Fairchild's proposed construction would limit the invention to planar-gate power MOSFETs, in violation of the well-established rule prohibiting claim constructions that would exclude preferred embodiments.

Fairchild proposes to add a limitation not present in the disputed claim language: "corresponding to the plurality of areas of the mask which are not open." It appears that Fairchild's proposed claim language is intended to exclude trench gates on the theory that they are defined by the etching in the area of the mask that is open. As noted above, in a trenched-gate power MOSFET, the gates are defined by the distance the polysilicon is etched downward into the substrate beneath the opening in the mask, rather than by the width of the mask used to etch the polysilicon. In fact, the mask exposes the gate material in the trenched gates to etch away excess material, thus defining the vertical dimension of the gate. *See* '630 patent, Fig. 6; Salama Decl ¶ 7. Because Fairchild's proposed construction excludes a preferred embodiment from the '630 patent's specification, it should be rejected. *See Vitronics*, 90 F.3d at 1583.

To support its proposed exclusion of trenched gates from the claims, Fairchild misleadingly cites only the figures in the '630 patent that depict planar-gate devices, and cites

only the language in the specification that provides a detailed description of planar-gate devices. Wu Ex. 11, *see* Joint Claim Construction and Pre-Hearing Statement, Ex. B at 5.

The specification expressly includes trenched gate structures. First, Fig. 6 depicts a trenched-gate MOSFET device, and the specification states that Fig. 6 is a view "of a trenched MOSFET device of the present invention." *Id.* at col. 5:44-45. In particular, Fig. 6 depicts the teachings of the patent: it shows the shallow and deep high-concentration body-dopant regions (region 260, labeled SP+, and region 265, labeled DP+), and the removal of a top portion of the substrate (silicon etch of depth δ). Second, the specification at cols. 8:55-9:17 describes the formation of a trenched-gate MOSFET device, with particular emphasis on the shallow and deep high-concentration body-dopant regions. Because the process of etching to define gates is well-known, the patent need not repeat it. *Spectra-Physics, Inc. v. Coherent, Inc.*, 827 F.2d 1524, 1534 (Fed. Cir. 1987) ("[a] patent need not teach, and preferably omits, what is well known in the art."). Fairchild's attempt to exclude all trenched-gate MOSFETs from the coverage of the asserted claim improperly ignores all of this intrinsic evidence. It also violates the rule, adverted to above, prohibiting constructions that would exclude a preferred embodiment.

The Court also should reject Fairchild's proposed definition because it is inconsistent with the plain language of the claims. Etching can define either horizontal or vertical dimensions of device elements. Salama Decl. ¶ 7. There is nothing inherent in the words "etch" or "define" that would limit their use to horizontal dimensions. Salama Decl. ¶¶ 3-5, 7.

D. The '776 Patent

1. Background to the '776 patent

The invention of the '776 patent made possible power MOSFETs having a lower threshold voltage, V_{TH}, resulting in faster, more efficient devices without compromising reliability. As discussed below, the inventors of the '776 patent came up with a design in which the doping concentration of material in a particular part of the current path in the device was reduced, thereby reducing the amount of charge that must be overcome to turn on the device.

Power MOSFETs include regions (e.g., source, body, drain) having opposite conductivity types. Typically referred to as n-type or p-type, "conductivity" indicates whether a region of the

transistor carries an excess of Negative charge carriers (electrons) or Positive charge carriers ("holes"). This excess of charge carriers is typically achieved through "doping" the underlying silicon material with a dopant such as arsenic or boron. The doping concentration is often labeled with a "+" or "-" to indicate heavily or lightly doped regions. A region of one conductivity type is "compensated" if impurities of the opposite conductivity type are put into the region to reduce its doping concentration. Salama Decl. ¶ 8.

2. The invention of the '776 patent

Prior art trenched-gate power MOSFETs had inherently high threshold voltage, V_{TH}, that was typically barely below the voltage of the power supply used in many applications. '776 patent, at col. 2:8-20. Such prior art devices were unsuitable for certain low power applications, such as low power applications using batteries, which drop in power over time. *Id.* Prior to the invention of the '776 patent, prior art attempts to reduce the threshold voltage resulted in lower production yield (more devices fail to work properly) or less reliable devices (more devices fail during use). '776 patent, col. 2:42-51. Another consideration was prevention of a phenomenon known as "punch-through." When punch-through occurs, a current-conducting channel is formed in the body region between the source and drain even if no voltage is applied to the gate. As a result, current flows between the source and drain even when the MOSFET is supposed to be off. The '776 patent describes how prior art attempts to reduce threshold voltage resulted in low punch-through tolerance. *Id.* at col. 2:52-col. 3:23.

The '776 patent teaches a method of reducing the threshold voltage of a power MOSFET device without sacrificing production yield or reliability of the devices, and without compromising punch-through tolerance. The '776 patent achieves this goal by "compensating" a portion of the body region adjacent the source region with dopants whose conductivity type is the opposite of the conductivity type of the body region. *Id.* at col. 3:50-58. For example, if the body region is p-type and the source region is n-type, the invention of the '776 patent includes compensating a portion of the body region adjacent to the source region with n-type dopants. Salama Decl ¶ 8. This compensation is accomplished by "ion implanting" dopants into the silicon material, *i.e.,* bombarding the silicon structure with atoms or molecules of the dopant.

'776 patent, at col. 5:48-61. Because of the reduced overall charge in the compensated portion of the body region, less voltage is required to turn on the device, and the threshold voltage of the device is reduced. *Id.* at 58-61.

Claim 1 of the '776 patent recites as follows:

> 1. A method of forming a semiconductor structure comprising the steps of:
> (a) providing a substrate having a major surface;
> (b) forming at least one trench in said substrate;
> (c) forming a body region of a first conductivity type in said substrate, said body region having a diffusion boundary in said substrate;
> (d) forming a source region of a second conductivity type in said body region; and
> (e) compensating a portion of said body region by implanting material of said second conductivity type in said body region, said portion being proximal to said source region and spaced from said diffusion boundary of said body region and said major so as to reduce the impurity concentration of said first conductivity type in said portion of said body region.

Wu Decl., Ex. 2. The disputed claim language is highlighted. The same claim language appears in claims 13 and 25, which are also asserted by AOS.

3. "Compensating a portion of said body region by implanting material of said second conductivity type in said body region"

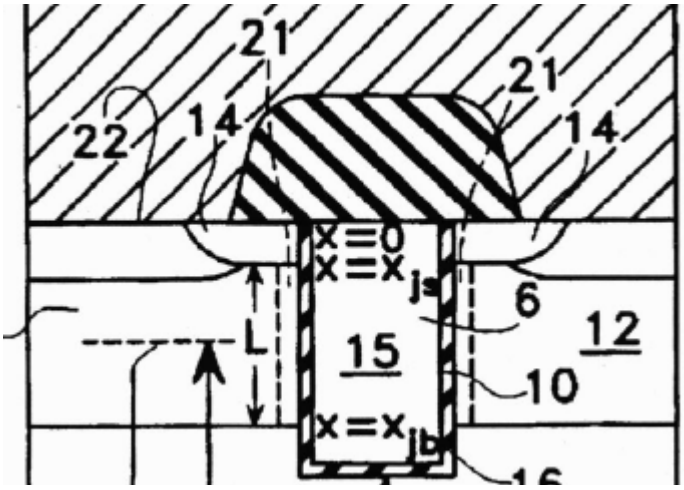
Disputed Term	AOS's Proposed Construction	Fairchild's Proposed Construction
Compensating a portion of said body region by implanting material of said second conductivity type in said body region	**Implanting into the body region material having conductivity type opposite the conductivity type of the body region.**	**Implanting impurities of the second conductivity type into the body region such that the peak concentration of that implant is located in the body region, and such that the conductivity type at the location of the peak concentration of that implant does not change.**

AOS proposes a construction for this claim element that simply tracks the plain language of the claim: implanting material of the opposite conductivity type into the body region. Fairchild seeks to incorporate two additional limitations regarding "peak concentration" into this straightforward claim language. These additional limitations are without support in the claim

language, specification, prosecution history, or any other evidence identified by Fairchild.

The specification of the '776 patent explains the process of compensating a portion of the body region in multiple locations. *See, e.g.*, '776 patent at Abstract; col. 3:55-58 ("A predetermined portion of the body region adjacent to the source region is *compensated* in impurity concentration by ion implanting a material of the second conductivity into the body region.") In the diagram to the right (from the '776 patent), 14 is the source, and 21 is the channel (which is part of the body 12). The portion that is compensated is near the top of the channel, roughly where the dotted line from 21 ends. As the specification states, compensation involves ion implanting impurities into the body. The implanted impurities have conductivity type opposite that of the body region. This is exactly the definition proposed by AOS.

Moreover, the '776 patent uses the term "compensating" with the standard meaning in the art. For example, the IEEE Standard Dictionary of Electrical and Electronics Terms (6th ed. 1997) defines "doping compensation" as "[a]ddition of donor impurities [i.e., n-type] to a p-type semiconductor or of acceptor impurities [i.e., p-type] to an n-type semiconductor." Wu Decl. Ex. 7 at 313. This Sixth edition of the IEEE Standard Dictionary was published in 1997, the same year the application for the '776 patent was filed. *Id.* The Wiley Electrical and Electronics Engineering Dictionary (2004) defines "compensated semiconductor" as "[a] semiconductor with two types of impurities or imperfections, in which the electrical effects of one type of impurity or imperfections partially cancels the other. For instance, a donor impurity partly annulling the electrical effects of an acceptor impurity." Wu Decl. Ex. 10 at 130. *See also* Wu Decl. Exs. 8, 9. All of these highly-regarded technical dictionaries show that the essential feature of compensating is adding impurities of opposite conductivity type. Salama Decl. ¶ 8. This is the same meaning applied in the specification and proposed in AOS's definition.

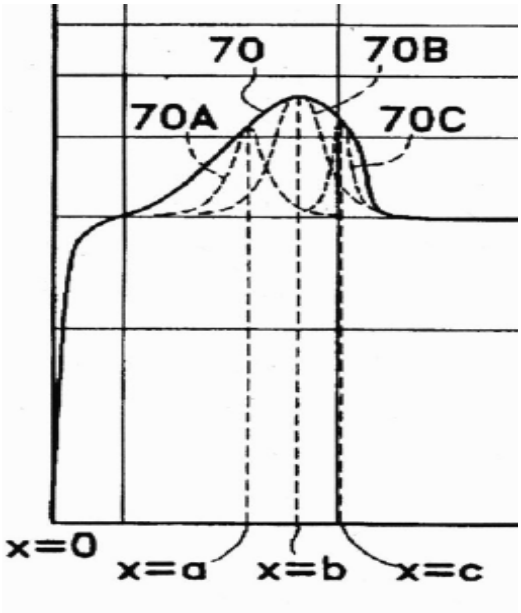


a. Fairchild Proposes to Impose Additional Limitations Based on "Peak Concentration"

The phrase "peak concentration" does not appear anywhere in the specification of the '776 patent. Neither the specification nor the claim language include any statement or suggestion that the "compensating" step of claim 1 requires that "the peak concentration of that implant is located in the body region," or that "the conductivity type at the location of the peak concentration of that implant does not change."

Nor has Fairchild identified any other evidence supporting its proposed limitations. Technical dictionaries and treatises that define compensation do not refer to "peak concentration" or any similar phrase. Fairchild has not identified any references that support its construction, and an extensive investigation of technical resources yielded none that included "peak concentration" in the definition of compensation. *See, e.g.*, Wu Decl. Exs. 7-10.

Moreover, the '776 patent specification refutes Fairchild's proposed limitations. To understand Fairchild's proposed definition and how the example refutes it requires a brief overview of the process of ion implantation.



Ion implantation involves bombarding a target with energized ions. Salama Decl. ¶ 9. The greater the energy of the ions, the greater the penetration into the target. Salama Decl. ¶ 9. See also '776 patent at Fig. 6 (showing the relationship between ion energy and penetration distance for arsenic (As), Phosphorus (P), and boron (B)). Due to random collisions, ions of the same energy penetrate the target to varying depths. See, e.g., '776 patent at Fig. 5, a portion of which is shown at the right. Dotted curve 70B shows the varying depths of the implanted ions with average depth of b. The distribution of depths is much like the distribution of scores on a standardized test (a "bell curve"). The bell curve of depths has a peak where the highest number of ions penetrate. This is

the depth that Fairchild refers to as the "peak concentration."

Fairchild proposes that a region is not compensated unless the "peak concentration" of the implant is in that region. For example, if the "peak concentration" of an implant is in the source region rather than the body, then Fairchild would say that the body region has not been compensated. Regardless of how many ions have been implanted into the body region and cancelled the impurities in the body region, Fairchild asserts that there is no compensation unless the "peak concentration" is in the body region.

Not only is Fairchild's proposed definition implausible, it is contrary to the teaching of the '776 patent specification, specifically, Figure 4 and Figure 5 and corresponding description at col. 5:48-54 and col. 7:40 – 8:4. In Figure 4 and Figure 5, the horizontal axis (labeled as "DISTANCE") is the depth within the substrate, with the top of the substrate to the left (x = 0) and the bottom of the substrate to the right. In Figure 4, the region to the left of $x=x_{js}$ is the source region, and the region to the right of $x=x_{js}$ is the body region. '776 patent, col. 5:19-22. Curve 64 represents the doping concentration in the source region, curve 66 represents the doping concentration in the body region, and the vertical dotted line at $x = x_{js}$ shows where the source meets the body. Dotted curve 30 shows the overall doping prior to the compensation step. *Id.* at col. 5:22-36.

The three dotted curves 70A, 70B, and 70C in Figure 5 represent three implants at depths a, b, and c, respectively. According to the specification, these three implants together produce compensation curve 70, *i.e.,* each is a compensation step. *Id.* at col. 5:48-61. Under Fairchild's proposed definition, however, step 70C does compensate the body, but 70A does not because the "peak concentration" of implant 'a' is in the source region. Since 70A is in the source region, Fairchild's proposed construction is therefore directly at odds with the specification.

IV. CONCLUSION

For all the foregoing reasons, AOS's proposed constructions should be adopted.

Dated: March 13, 2008

MORGAN, LEWIS & BOCKIUS LLP

By /s/ Daniel Johnson, Jr.
Daniel Johnson, Jr.

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GENERAL ORDER ATTESTATION

Pursuant to General Order No. 45, Section X(B) regarding signatures, I, Andrew J. Wu attest that concurrence in the filing of this document has been obtained from Daniel Johnson, Jr. I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Executed this 13th day of March, 2008, at Palo Alto, California.

/s/ Andrew J. Wu
Andrew J. Wu